REMARKS

Claims 1-2, 4, and 6 have been amended. Claims 7-14 have been added. Claims 1-14 are all the claims pending in the application.

Formal matters

Applicant thanks the Examiner for accepting the drawings as filed on July 15, 2003, and for acknowledging claim to foreign priority and receipt of a certified copy of the priority document. Applicant also thank the Examiner for reviewing and initialing the documents in the Information Disclosure Statement submitted on July 15, 2003.

Allowed claims

Applicant thanks the Examiner for allowing claims 3 and 5.

Claim Rejections -- 35 U.S.C. § 112

Claims 2, 4 and 6 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant has amended the claims and respectfully requests that the Examiner withdraw the rejection.

Claim Rejection -- 35 U.S.C. § 103

Claims 1 and 2 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,628,256 to Nishimura in view of U.S. Patent No. 4,823,120 to Thompson. Applicant respectfully traverses this rejection.

As an initial matter, Nishimura and Thompson are not combinable. Nishimura is directed to drive circuits for liquid crystal displays. Specifically, Nishimura is concerned with overcoming the limitations caused by both increasing clock frequencies and increased bus width. As the clock frequencies and bus widths increase, the amount of change in the value of each bit of data becomes larger. This increases the power consumption of the drive circuit. Moreover, wider bus lines operating at higher frequencies also increase the electromagnetic interference noise that is radiated due to higher rate of change of the data on the bus lines. Wider buses also increase the incidence of cross-talk between data lines of the bus. Nishimura seeks to address these problems and to reduce the amount of change in the values of each bit of data transferred over the bus lines.

By contrast, Thompson is directed to an enhanced video graphics controller for converting digital RGB digital signals to composite or analog output signals. Specifically, Thompson seeks to address constraints in computer memory and processor speed and to provide a larger variety of colors and update the video information at a higher rate.

One faced with the problems of Nishimura, i.e. eliminating electromagnetic interference and cross-talk on increasingly wider and faster bus lines, would not look to Thompson for a solution. First, Thompson ultimately involves outputting a composite or analog signal, whereas Nishimura works with digital signals -- video signals and bus lines. Second, Thompson is concerned only with converting RGB data to an analog signal, which may then be output by some other undisclosed process to the display. In other words, Thompson provides the signals to

apply to a drive circuit. Thus, Nishimura and Thompson are not combinable for at least these two reasons.

Even assuming *arguendo* that Nishimura and Thompson may be combined, the combination still does not teach all of the claimed features. For example, claim 1 recites the feature that the input video data is composed of parallel data as partially serialized output video data. The Examiner admits that Nishimura does not disclose the serialization feature, but argues that Fig. 2 of Thompson makes up for the deficiency of Nishimura. However, Applicant respectfully disagrees with the Examiner's position.

Fig. 2 of Thompson shows an input 16-bit data bus broken down into an 8-bit even word and an 8-bit odd word. These inputs are processed by new video mode pipeline 31 into a 12-bit word and a 4-bit address, which are then stored in RAM 19. A similar path through current video mode pipeline 38 performs the same procedure on RGB 8421 data. Both data are then fed into 24 bit latches 18 and then into multiplexer 17 which multiplexes the data. The output of the multiplexer 17 is fed into digital to analog converters 35. Thus, Thompson does not disclose partially serialized output video data as required by claim 1. Rather, Thompson is merely clocking parallel data out and then converting it to analog signals using D/A converters.

Therefore, claim 1 is patentable over the Nishimura and Thompson combination for at least the above-mentioned reasons.

Moreover, even assuming *arguendo* that Nishimura and Thompson are combinable, the combination still does not teach or suggest all of the features of claim 2. For example, claim 2

recites input video data of a 3 X 2n-bit parallel in a 2m-bit unit. The Examiner argues that this feature is taught by Nishimura in Fig. 4. At Fig. 4, Nishimura shows a set of laches 13-1 to 24 for clocking data into polarity inversion circuit 12 and further clocking out the data through another set of laches 14-1 to 24. Thus, Nishimura does not show, teach or suggest a 2m-bit unit, as required by claim 2. Moreover, Thompson does not cure this deficiency. As discussed above, Thompson merely shows clocking out parallel data through a multiplexer and D/A converters to form an analog signal. Thus, claim 2 is patentable over the Nishimura and Thompson combination.

New claims

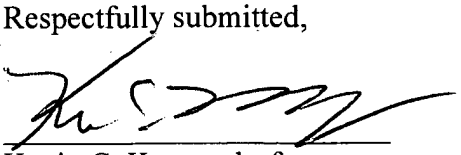
Applicant has added new claims 7-14 in order to claim additional features of the invention.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



Kevin C. Kunzendorf
Registration No. 58,308

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

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23373
CUSTOMER NUMBER

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